LISTING OF THE CLAIMS

What is claimed is:

1. (currently amended) A debugging system, comprising:

an integrated circuit chip comprising a processor constructed to execute a ~~software~~ program and to generate results data;

a data path constructed to transfer data from the processor;

a fast-response circuit coupled to ~~a low-level asset in~~ the processor;

the fast-response circuit configurable to extract sustained evidence ~~selectively~~ data from ~~the low-level asset without major time distortion of~~ the ~~software~~ program executing on the processor; and

wherein the ~~a~~ data path is constructed to both 1) transfer the extracted sustained evidence data to an off-chip location; and 2) to transfer the results data from the processor to an off-chip location ~~to an evidence file~~.

2. (currently amended) The ~~A~~ debugging system according to claim 1, ~~comprising:~~

~~a processor constructed to execute a software program;~~

~~a fast-response circuit coupled to a low-level asset in the processor;~~

wherein the fast-response circuit is configurable to monitor program execution ~~selectively sustained data from the low level asset~~ for a predetermined event without interfering with ~~major time distortion of~~ the ~~software~~ program executing on the processor; and

wherein the fast-response circuit is constructed to provide ~~transmit~~ an action signal responsive to the event.

3. (currently amended) The ~~A~~ debugging system according to claim 1, ~~comprising :~~

~~a processor constructed to execute a software program;~~

~~a fast-response circuit coupled to a low-level data asset in the processor;~~

wherein the fast-response circuit ~~having~~ has a first portion that is configurable to monitor the program executing on the processor ~~data from the low level asset~~ for a predetermined event, and is constructed to provide ~~generate~~ an action signal upon the occurrence of the predetermined event; and

wherein the fast-response circuit ~~having~~ has a second portion that is responsive to the action signal, and is configurable to ~~extract~~ selectively extract sustained evidence data from the program executing on the processor ~~data path low-level asset, and constructed to act responsive to the action signal~~; and

wherein the ~~a~~ data path is constructed to ~~transmit~~ transfer the extracted sustained evidence data to an evidence file without ~~major time distortion of~~ interfering with the ~~software~~ program executing on the processor .

4. (currently amended) The debugging system of claim 1~~, 2, or 3,~~ wherein the fast-response circuit ~~low-level asset~~ is constructed ~~as~~ to extract ~~the~~ evidence data from a commit buffer, a reorder buffer, a high speed data bus, or a register.

5. (currently amended) The debugging system of claim 1~~, 2, or 3,~~ wherein the fast-response circuit is integrated on-chip with ~~the low-level asset of~~ the processor.

6. (currently amended) The debugging system of claim 1~~, 2, or 3,~~ wherein the fast-response circuit comprises high speed registers.

7. (currently amended) The debugging system of claim 1~~, 2, or 3,~~ wherein the data path comprises one or more resources of the processor's hierarchy and use of the data path is shared by both 1) results data and 2) evidence data.

8. (currently amended) The debugging system according to claim 1 ~~3~~, wherein ~~further including~~:

sequential logic is connected to ~~first portion of~~ the fast response circuit; and

~~wherein~~ the sequential logic is programmable to ~~selectively~~ monitor ~~for~~ program execution for a predetermined event, and the sequential logic enables an action responsive to the ~~software~~ program event.

9. (currently amended) The debugging system according to claim 1 ~~3~~, wherein ~~further including~~:

sequential logic is connected to ~~first portion of the~~ fast response circuit; and

the sequential logic is programmable to selectively extract evidence ~~execution results~~ data ~~from the data path~~.

10. (original) The debugging system according to claim 8 or 9, wherein the sequential logic is constructed as a co-processor.

11. (original) The debugging system according to claim 8 or 9, wherein the sequential logic is integrated on-chip with ~~the low-level asset of~~ the processor.

12. – 18. (cancelled)

19. (currently amended) A debugging system, comprising:

a processor constructed to execute a ~~software~~ program and to generate execution results data; ~~and having~~

a ~~shared~~ high-speed data transfer path ~~bus~~ that:

is constructed to transfer execution results data, and

is in communication with an external data transfer bus and a file;

a reporter circuit comprising a fast-response circuit coupled to the high-speed data transfer bus and coupled to ~~a low-level asset in~~ the processor;

the fast-response circuit configurable to extract sustained evidence data from the program executing on the processor in response to detecting a predefined event ~~low-level asset~~; and

a scribe constructed to transfer the extracted sustained evidence data through the high-speed data path ~~extending~~ to an evidence file ~~, the high-speed data path in communication with an external including the shared high-speed data transfer bus~~.

20. (previously submitted) The debugging system according to claim 19, wherein the high-speed data path further includes one or more resources of the processor's hierarchy.

21. (currently amended) The debugging system according to claim 19, wherein the fast-response circuit is constructed to extract the sustained evidence data without interfering with execution of ~~the operation of major time-distortion to~~ the ~~software~~ program ~~executing~~ on the processor .

22. (currently amended) The debugging system according to claim 19, wherein the high-speed data path is constructed to transfer the sustained evidence data to the evidence file without interfering with execution of ~~the operation of major time-distortion to~~ the ~~software~~ program ~~executing~~ on the processor .

23. (new) The debugging system according claim 1, wherein the fast-response circuit is constructed to test for or to extract a branch destination from the program execution.

24. (new) The debugging system according claim 1, wherein the fast-response circuit is constructed to test for or to extract a time-stamp from the program executing on the processor.

25. (new) The debugging system according claim 1, wherein program execution results are substantially unchanged whether or not the fast-response circuit extracts evidence data from execution of a given program.

26. (new) The debugging system according claim 1, wherein program execution and evidence transfer occur substantially simultaneously.

27. (new) The debugging system according claim 1, wherein program execution with evidence extraction and transfer occurs with a time distortion ratio that is less than 3X.

28. (new) The debugging system according to claim 1, wherein the off-chip location is a data file.

29. (new) The debugging system of Claim 1 wherein the data path includes a communication link.

30. (new) The debugging system of Claim 7, wherein the resources of the processor's hierarchy includes a data path associated with the processor's hierarchy.

31. (new) The debugging system of Claim 7, wherein the resources of the processor's hierarchy includes a memory associated with the processors' hierarchy.